Optical Interconnects in Conventional Electronic Computers

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ABSTRACT

Optical interconnections have become the medium of choice for the long haul communication. As the speed of the modern day computers are increasing, the speed of data transfer may reach a limit. This creates a motivation to replace electronic buses with all optical ones. Several avenues of research have emerged in optical interconnects for digital systems. In systems architecture level studies, the goal is to understand the role of the different levels of interconnection hierarchy within digital systems in the overall performance equation. Another avenue of studies identify active and passive components that will be most suitable to implement optical interconnects. These components are used to design the physical organization, the communication protocol in the existing computer architecture. Another type of studies may propose modification of the existing computer architecture, which can take advantage of the high bandwidth, multi-wavelength, ultrafast optical communication and various advancement in long haul optical communication.

Keywords: optical interconnects, digital systems, computer bus, board-to-board, backplane, box-to-box, parallel computing, optical backplane, interconnection hierarchy, computer systems design computer architecture, active and passive components.

1. INTRODUCTION

The objective of this paper is to review the trends of optical interconnection studies for digital systems [1]. Mainly two types of studies emerge in the area of optical interconnects for digital systems [2]. One type of studies attempts to establish the fact that it is indeed possible to replace the electrical interconnections with optical ones. The historic reason for such an approach comes from optical computing area, where there is a late trend of doing what electronics can do better in electronics and utilizing optics where optics has an edge over electronics [3,4]. Naturally, optics has already proven its superiority in communications as evidenced by the success of high bandwidth high data-rate long haul optical communications.

The former studies concentrate on active and passive components that can become the building block of interconnections, which exist at different levels of interconnection hierarchy in a digital system or a computer [5]. These levels are namely inter-chip, intra-chip, bus level, backplane level, board-to-board, and box-to-box. In each of these levels, the components may be different, because requirement varies from level-to-level and hence solutions must also differ. However, it is also noted that as we go from shorter to longer distances more solutions are readily available, a consequence of the very mature yet rapidly expanding field of (fiber) optic communications.

However, a system cannot be expected to improve by changing merely one component or a specific type of interconnections. The second type of studies of "optical interconnects for digital systems" concentrate on the system architecture level studies [5] where the appropriate timing parameters are analyzed [7] to quantify the overall impact of optics and hence justify the usage of optics in the overall architecture of the computer. Both types of studies get its impetus from the success of fiber optic communication [8].

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Apart from these two major trends, a third type of studies can be envisioned which says that it is possible to replace these electrical conductors by optical ones (as a result of the first type of study), however, systems studies point out that it may have greatest impact on performance if certain aspect of the architecture or systems design can be modified [9,10]. Such studies could be called optoelectronic systems design.

2. COMPONENTS FOR DIGITAL INTERCONNECTIONS

In a computer, interconnection exists inside a chip, between various VLSI modules; also they exist between individual chips on a board. Ultimately, all boards are connected to a backplane, which performs board-to-board interconnection. Multiple computers can also be interconnected in a distributive computing environment. Depending on various layers of interconnection hierarchy, they can be divided into the following:

(a) very short distance intra-chip (less than one or several centimeter)
(b) short distance chip-to-chip (centimeter to meter)
(c) Medium distance backplane or board-to-board
(d) Long distance box-to-box

It should be stated here that the division above attempts to go from very short to long distance. In a sense, each of these can be seen as systems itself. For example, for intra-chip, we must first quantitatively evaluate the pros and cons of using optical connections inside a chip [3,4]. However, it differs from the second type of studies [6] in the sense that there we are dealing with multiple components of a computer and their interaction leading to a single performance parameter which is far complex than increasing the communication speed or number of channels inside a chip.

Although component studies concentrate on the actual hardware; nevertheless, they justify their work by attempting to optimize certain aspects of the hardware. These could be amount of actual hardware, clock skew etc. Three types of technology are involved in creating the physical layers: optical source and detector or opto-electronic transceiver, optics (which includes the passive components) and opto-mechanical packaging (which gives the complete system). We now look into (a) active and (b) passive components suitable for digital optical interconnectios.

2.1. Passive Component: physical Media

Different kinds of fibers are available currently. Single mode glass fibers (SMF) have traditionally been used in the telecommunication, extending from trunks to access applications. The core size of SMFs usually varies from 8 μm to 10 μm. Connectivity cost is expensive and SMF is usually recommended for longer distance and higher bit-rate transmission. On the other hands, Multimode fibers are considered to be used in comparatively shorter distance. As a physical media, multimode fibers, especially fibers with larger core diameter are indispensable, which should yet to be cost-effective, and easier to handle. In that respect, plastic optical fiber (POF) is considered to be the best candidate for the computer system interconnections and others short distance interconnection, where distances varying from 1m to 100m. POF's core diameter varies from 0.25 mm to 0.98 mm whereas core diameter of multimode silica fibers varies from 0.05 mm to 0.2 mm. PMMA based POF has lower attenuation at 650 nm and with doping of fluorine (CYTOP POF) [11] the lower attenuation window can be extended to longer wavelength, as shown in Fig.1. Standard PMMA based step-index POF can handle the data rate of >1 Gb/s at the distance of 10m. With higher bandwidth demands, graded-index (GI) - POF could handle multigiga-bit data transmission. Recently, CYTOP based GI-POF could enable to handle further higher bandwidth [12]. Graded index glass fiber of larger core diameter can also be used in computer networks.

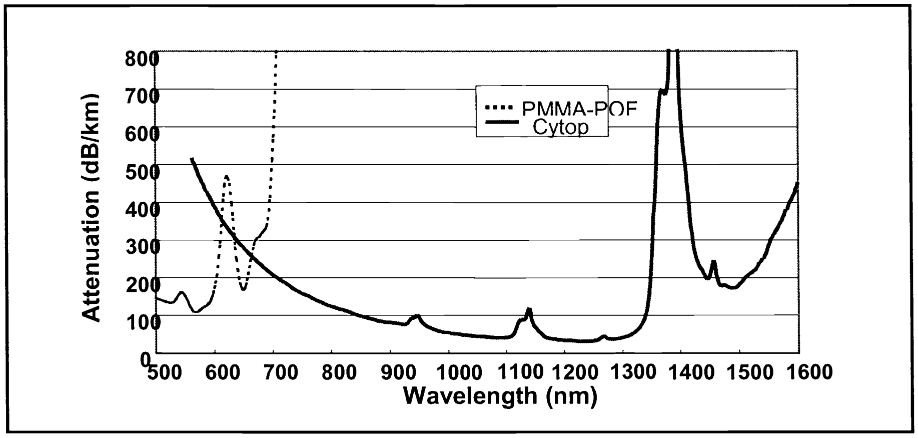

Fig. 1. Spectral attenuation of POFs

In the case of parallel data transmission, ribbon fiber made from plastic, or image fiber, especially made from the glass, can be used in the board-to-board and/or box-to-box interconnection. These fibers can reduce the level of effort required to install, configure and manage Fiber Optic Network. Ribbon fiber optic systems reduce the cost of labor and require no special tools or expensive test equipment to install fiber optic backbone infrastructures. Standard available connectors such as MTU, RT-45 etc. can be used to connect the array ribbon fiber, which could save the space in the backplane. Another types of fiber that could be installed on the wide area of plastic surface are the flexible fiber, usually named in the industry as the flex optical circuit. This provides one of the highest density and versatile interconnect systems on the market today. For high fiber count interconnects in backplanes and cross-connect systems, the high density routing on a flexible, flame-resistant substrate provides a manageable means of fiber routing from card-to-card or shelf-to-shelf. Figure 2 shows the optical flex-circuit for the board-to-board interconnection. Polymer based interconnections has also been used for board level 2-D planar waveguide circuit [13,14].

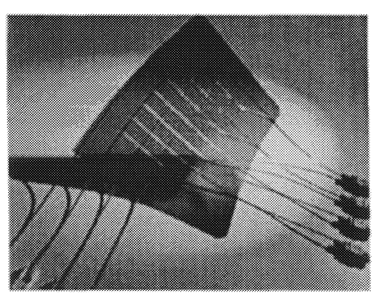

Fig. 2. Flex fiber circuit for high-density backplane interconnection.

In the case of the chip-to-chip interconnection, the silica, polymeric [15] or plastic waveguide [16,17] could be used. Complex waveguide networks could be fabricated using conventional Si-technologies. Recently, significant low loss silica waveguide has been demonstrated using the APCVD technologies [18,19,20]. As the optical devices such as the LED or LD and photodetector (PD) cannot be fabricated from the same Si materials, the silica waveguide network fabricated from Si technologies along with Si-IC could help significantly to couple the optical signal to/from the optical devices fabricated from the separate materials such as InP or GaAs compound semiconductors, and help to maintain chip speed. Hybrid technologies using the common Si substrate would be used for this purpose. This technology is becoming matured in the telecommunication arena, which is expected to reduce the optical device cost and also produce optical devices with high functionality. These would be explained later in the optical devices sections.

2.2. Optical Devices

As the standard POF has a lower attenuation at the vicinity of 517 nm and 650 nm, the use of optical source at those wavelengths can be used for short distance interconnection such as computer network computer [21]. Currently, 650 nm material technologies are much matured than 517 nm, and for this, as a transmitter source for Home and Office network application, 650 nm light emitting diode (LED) and laser diode (LD) could be used. Figure 3 shows the dependencies of transmission speed on fiber types and source. The required transmission capacity dictates the fiber and optical source technology being used. The 650 nm LED could be used in such an link application that 100 m data transmission at 156 Mb/s is required, whereas LD could be used in a link application that giga-bit-rate data transmission through 100 m or more. Table I summarizes the light sources required for very short interconnection. The LED could support < 1Gb/s interconnection in the backplane. To achieve higher speed, first consideration is to be concerned on suitable optical sources. Laser source can provide higher speed. Based on the physical media, 650 nm LD or 980 nm can offer multi-gigabit range data rate in cost-effective way.

2.2.1 Optical Sources

650 nm Surface-Emitting LED

As an optical source, surface emitting type LED of 650 nm is an attractive alternative to the LD due to its potential for eye safety and also for low-cost interconnection. Besides, LED has longer run reliability at any environmental condition, very much suitable in the backplane interconnection. The structure of LED

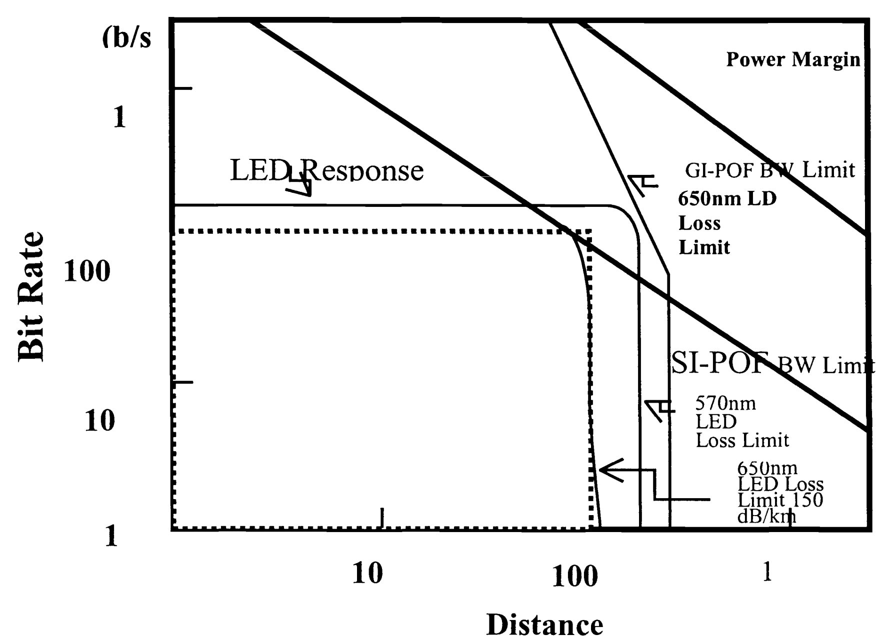

Fig. 3. Dependencies of transmission capacity on selection of fiber types and sources.

Table: I. Summarizes the optical cost-effective transmitter sources available for back plane interconnection

Available Optical Sources
(Cost-effective)

Wavelength	Light	Modulation Speed
650 nm	DFB LD	> 1Gb/s
650 nm	LED	> 250 Mb/s
570 nm	LED	~ 10 Mb/s
1300 nm	FP/DFB LD	> 1 Gb/s

also determines the POF transmission performance [22-24]. Making smaller launching NA (numerical aperture) can transfer the data to longer distance, as the modal dispersion could be minimized [22]. Figure 4 shows the cross-sectional view of a surface emitting diode useful especially for POF data links. The use of bottom DBR can enhance the optical output over three times [25-28] as compared with the LED without DBR. The structure is grown layer-by-layer using the MOCVD with precise control of composition and structure. The precise control of p doping is also required to enhance the total optical efficiency. With

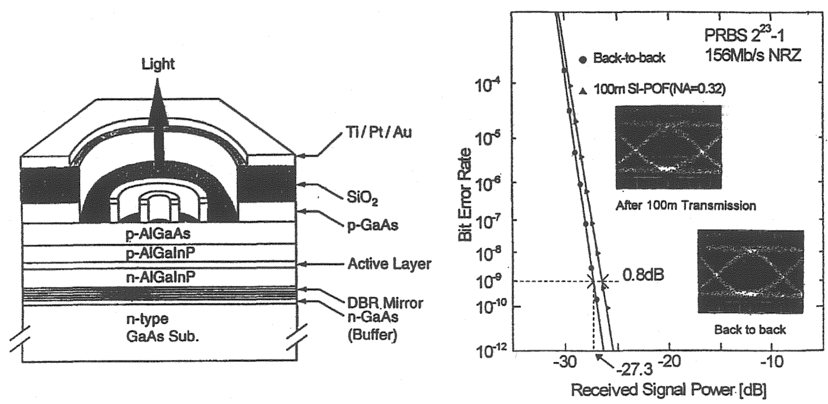

Fig. 4. 650 nm Surface Emitting Type LED: (a) Cross-sectional view, and (b) Transmission performance. Here, step-index POF of having NA (numerical aperture) of 0.32 was used for 100 m transmission experiment.

using the ring electrode along with the plastic lens, it is possible to reduce the launching NA to as low as 0.9, and achieve the coupling efficiency as high as 80% (NA = 0.32 and core diameter = 0.98 mm) [27]. Link performance after passing through 100 m POF at 156 Mb/s data rate, as shown in Fig. 4(b), indicates its compatibility for POF for comparatively short distance interconnection. Data rate at 600 Mb/s over 100 m POF transmission could also be possible using this LED and peaking circuit. Now, 150 Mb/s transceiver using 650 nm LED over SI-POF are available in market, and higher speed of 156 Mb/s, 250 Mb/s and 400 Mb/s are likely to be commercially introduced soon. Multi-gigabit speed below 10 m POF transmission distance can be expected, which indicates possible implementation of the POF in short interconnection.

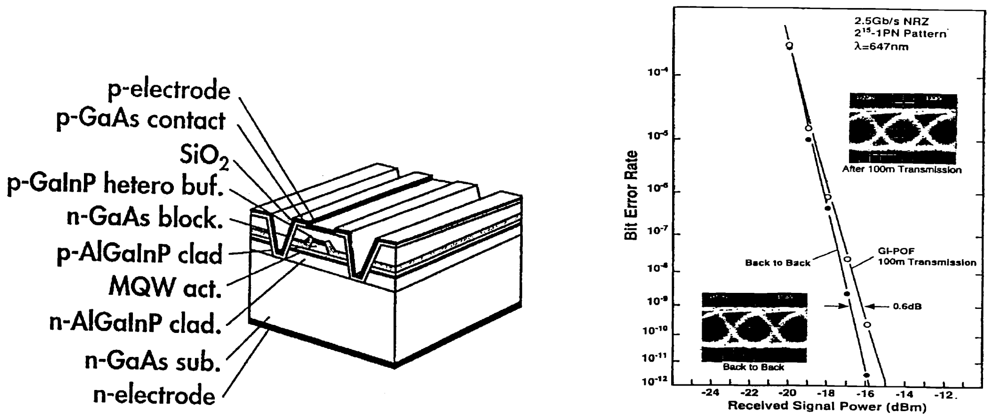

Fig. 5. 650 nm Edge-Emitting Type LD: (a) Cross-sectional view, and (b) Transmission performance. Here, graded-index POF was used for 100 m transmission experiment at the data rate of 2.5Gb/s .More higher speed data rate will be expected if the transmission distance get lower.

Edge-Emitting Diode

The 650 nm edge-emitting types LD could also be used in the POF data links where higher data rates, especially giga-bit-rate ranges are desired [28]. Figure 5 shows the cross-sectional view of 650 nm LD for GI-POF based data link. The structure is grown layer by layer onto GaAs wafer by MOCVD with precise control of composition, thickness, and uniformity. Standard III-V processing techniques are used for fabricating the LD. Conventional TO can package could be used for packaging the device, and inclined silicon platform could be used as a chip carrier for making the emitting beam upward, and focused to the fiber for link application. Link performance, as shown in Fig 5(b) indicated that 100 m transmission through GI-POF at the bit rate of 2.5 Gb/s could be possible, having power penalty of < 1 dB. Recent development of GI-POF using perflurine can extend its lower attenuation window from 500 nm to over 1300 nm, and also increasing its bandwidth. This makes it possible to choose wide variety of optical sources (650 nm, 780 nm, 850 nm, 980 nm, and 1300 nm). Recently, data transmission at 2.5 Gb/s and 11 Gb/s through 300 m and 100 m of perflurineted GI-POF, respectively have been demonstrated using 1300 nm LD [29,30]. This indicates the compatibility of POF links in short-distance high-speed link system. For higher bit rate (622 Mb/s to 2.5 Gb/s) and longer transmission distance (several km), 1300 nm LD is considered to be used with single mode glass fiber. As backplane would require very shorter distance varying 1 m to 10m, LD of wavelengths 650 nm or 1300 nm could be used for high-bit rate (~10Gb/s) backplane interconnection.

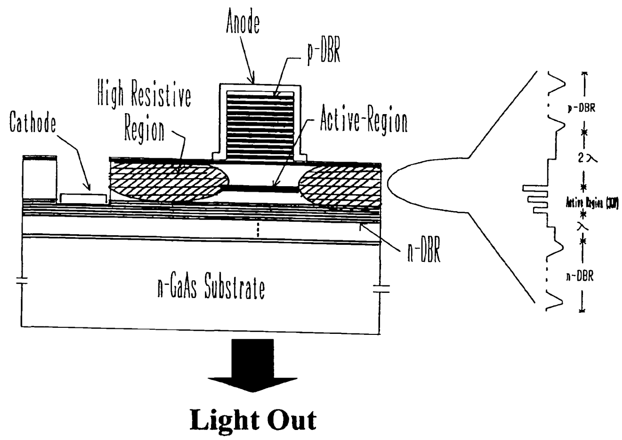

Fig. 6. Schematic of a 980 nm VCSEL.

Vertical-Cavity-Surface Emitting Diode (VCSELs)

VCSELs are cost-effective, highly reliable light source for gigabit data communication. Short wavelengths (850 nm and 980 nm) could be used to transmission distances of a few hundreds meters over multimode glass fiber. VCSELs are viewed as cost advantages and better performances over traditional edge-emitting LD. It offers circular output beam with a small divergence angle, fast modulation rates [31,32], high polarization controllability [33], stable performance over temperature [34], low threshold currents [35], wafer-scale fabrication, and 1-D and 2-D arrays. Figure 6 shows the cross-sectional view of a 980 nm VCSELs. The structure is grown layer by layer onto a wafer substrate typically by MOCVD, allowing precise control of layer thickness, composition, and uniformity. Device is then fabricated using III-V processing techniques. Critical features are formed by lithography, leading to high yield and high performances. As VCSELS are

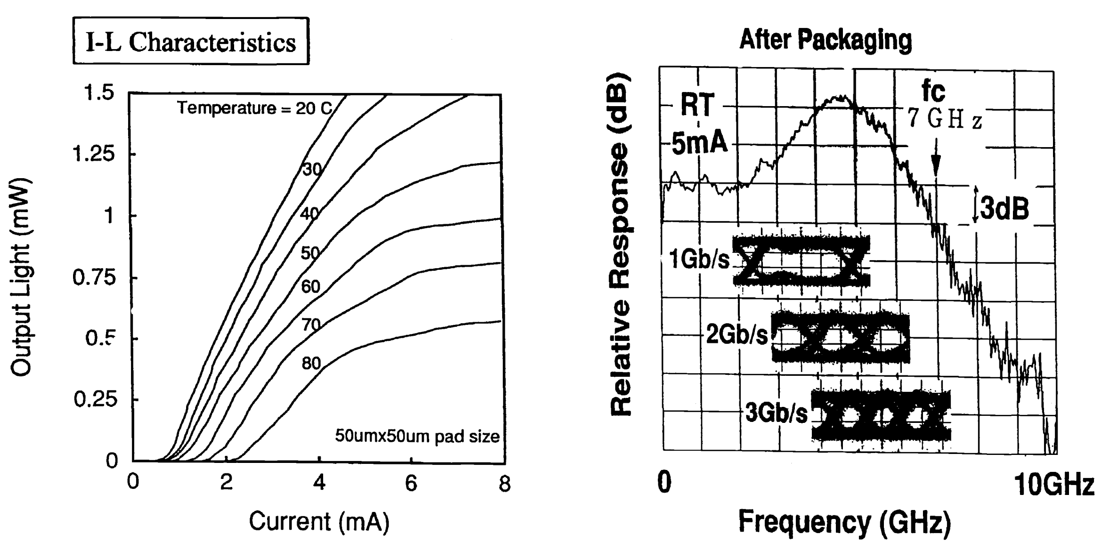

Fig.7. Performance of 980 nm VCSELs: (a) I-L characteristics, and (2) Frequency response characteristics.

surface emitters, wafer scale testing can be employed, resulting in lower packaging cost. VCSELs have also shown sub-milliamp threshold currents and also little variation with the temperature, as is shown in Fig. 7(a). It can also operate at high speeds with relatively low driving currents, as shown in Fig. 7(b). The insets show the back-to-back eye-pattern at different data-rate. 7 GHz bandwidth could be possible at 5 mA driving current. The low power consumption eases package design by reducing the heat problems. VCSELs also have good link performance through multimode fiber. Figure 17 shows the eye-pattern obtained after passing through plastic clad fiber (PCF) having 0.2 mm core diameter and NA = 0.4. Over 1 km transmission at the data-rate of 1.5 Gb/s could be possible, which indicates that VCSELs with large core PCF is also an other option extending the transmission distance to 1 km (which covers building backbone applications) at giga-bit-rate. Recently, successful demonstration of CW operation of 1300 nm VCSELs also gave a certain assurance of VCSELs probable future applications in comparatively for the short distance transmission in both plastic and glass fiber [36,37]. More work is still required to be done on 1300 nm and also 1550-nm VCSELs prior to implement in the interconnection applications

2.2.2 Planar Lightwave Circuit on Si-substrate:

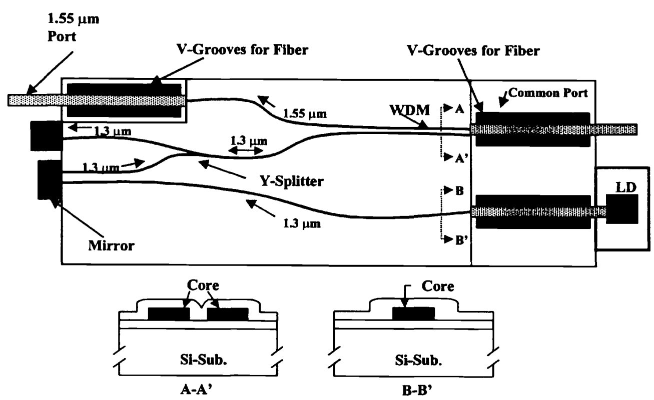

Fig. 8. Example of PLC based transceiver on Si-substrate for the short distance communication. Similar technology could be used for integrating the optical device for backplane interconnection especially chip-to-chip interconnection.

Figure 8 shows the example of the silica based bi-directional transceiver fabricated on the Si-substrate for access networks. For the chip-to-chip interconnection silica network on the silicon can be fabricated for interconnection purpose. Silica waveguide acts as optical guiding media. Common Si-process technology can be used for interconnection and chip together. Only for the optical devices such as the light source and detectors, hybrid technique can be used for integrating on the same chip. Hybrid technologies are getting matured in the telecommunication for fabricating higher functional optical device on the Si substrate [38,39]. Similar technologies can also be implemented for chip-to-chip interconnection. Only well-defined design [19] and precise controlling of process techniques could make the attenuation close/below to the glass fiber [20,21]. Fabricating V-grooves on Si substrate enables to align the fiber with the fabricated waveguide

3. COMPUTER SYSTEMS POINT OF VIEW

The performance of a computer is measured in terms of the execution time [7] of a computer program running in the system. The execution time depends on three factors: the instruction count (the number of instruction in a program), average execution time per instruction and clock cycle time. Obviously, to improve the performance we must reduce the execution time. One of the trends that most general users are familiar with, because of its widest publicity, is of course the clock cycle time. To understand the impact of interconnection speed on average execution time per instruction, we must look at the whole picture. What really happens in a single CPU non-pipelined computer? As we know computer is organized into three basic functions units: CPU, memory and I/O. CPU fetches the instruction, decodes it, executes it and then stores the result in some memory. (If we don't store the result in memory, what is the proof that any operation was done?). Now lets look at the fetching. How is it done? The CPU places an address on the address bus (how fast this address reaches the memory is of course a function of the bus speed, i.e., the interconnection between memory and CPU. Other handshake signal that comes before or after the address itself also is part of this time.) Now after a certain time, known as memory access time (again this is the most widely advertised memory parameter or memory speed) the instructions will be placed on the bus. During the memory accessing mechanism, the interconnection cannot do anything, it has to simply wait. Because this parameter, memory access time, is purely an electronic one, dependent only on the memory chip. When memory yields the instruction after the memory access time is elapsed, CPU reads the instruction into its internal buffer. Now the fetch cycle is complete. The decoding is CPU's internal business that the external bus does not interfere with. Thereafter the execution is purely a function of the CPU (or ALU) design (It is interesting to note that in earlier optical computing studies related to optical logic or bistability, one of the goals was to perform the execution at the speed of light, which is only *part* of the overall equation). A timing pattern similar to the instruction fetch will be carried out during the memory write. In brief, since instructions have to read to be executed, the average execution time is mainly limited by the memory access time, but not limited by the communication speed of the interconnection hardware. Again, an instruction can be pipelined where the instruction fetch, decode, execute and memory write operations are overlapped. Thus the execution time is not a simple formula where one can simply plug in the optical communication speed and get a simple answer.

The communication between CPU and memory cannot take place faster than the memory access time. A bus cycle, which involves the time taken by the CPU to read data or instruction must allow for the memory access time for reliable data transfer. Thus in that sense it does not matter how fast data can be moved between CPU to memory, the overriding fact is that memory speed not the communication speed is the bottleneck for overall computer systems performance.

This brings an interesting question, in a computer system, where maximum time is spent in the communication channel, will an optical communication infrastructure improve the overall system performance? Thus when multiple computers or multiple CPU must communicate with each other an optical backbone may have an advantage. For example using multiwavelength multiple units may communicate with each other at the same time using the same fiber backbone with tunable laser and detectors [9].

A parallel and distributed computing system may take advantage of optical interconnection. Optical fibers have shown to allow for a reduction of weight and volume compared to electronic ones [40]. Yoshikawa and Matsuoka [40] describe use of an optical interconnection in a parallel and distributed system. They use custom single chip LSI transceiver module for interfacing optical interconnection circuit with the electronic chips. The LSI logic includes 1.3 μm edge-emitting laser array and InGaAs pin photodetector array and laser driver. Laser drivers and receiver ICs were produced using Si Bipolar process. Collet et al. [6] discusses the role of optical interconnections in single and multiple CPU machines. For single CPU they suggest possible applications of optical interconnects between the lowest cache and the main memory, although competing electronic technology may provide upto 10 Gbyte/s connection in near future. For multiprocessor architecture the dominant factor is the network latency, which depends on the network topology and the overhead in routing and contention control. To find the network architecture which

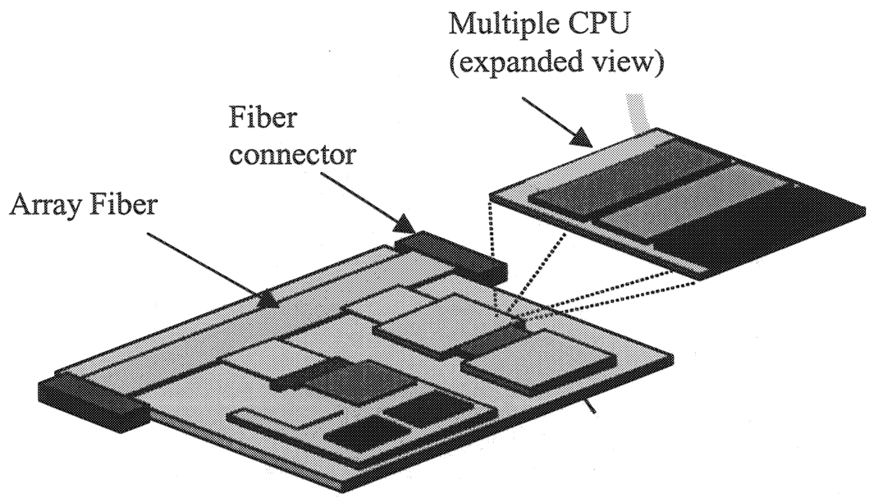

Fig. 9. Board-to-board and chip-to-chip interconnection scheme

provides the lowest network latency is a problem yet to be solved [6]. It may be possible to overcome or minimize the contention by using tunable laser sources and detectors. A possible chip-to-chip interconnection on a board is shown in Fig. 9, where array fiber is connected to chip set via transceivers. Also side connectors allow for connection to an optical backplane.

Another trend in implementing optical backplane is utilization of free-space interconnection. In such application, VCSEL and photodetectors are designed as transceivers. Holograms are [41,42] found suitable for coupling to and from backplane waveguide while microlens array may be used for collimation in order to reduce the cross talk between neighboring optical channel [43]. Cross talk, interconnection length and bit-error rate has been studied for board-to-board optical interconnects. The backplane proposed by Chen et al. [42] used VCSEL sources collimated by microlenses, which are coupled to the waveguide by means of holograms. The light diffracted into the waveguide travels in bi-directional fashion and is coupled (diffracted) into array of receivers again using the same hologram. Their work reports achieving 10^{-12} bit error rate. Since each outcoupling from the backplane reduces the energy, then the number of board that can be connected to the backplane will be limited. Alternately, one may think of amplifiers to increase the number of boards or length of backplane. The free-space interconnection has the problem of misalignment [44], which is not present when fiber coupling is used [40]. Other trend includes interconnecting processor in a pipelined fashion [45]. Smart pixel is another concept of designing transceivers with additional intelligence that could also be used in pipelined processor architecture or chip-to-chip interconnection [46].

4. CONCLUSION

Ultimately the success of long haul communication in increasing the speed and bandwidth may effect how this not-so-long distance communication takes shape. However, cost will be a prohibitive issue in incorporating optical communication into the computer. For example, in long haul communication, gain is provided say every 70km using erbium doped fiber optic amplifier. Now to provide gain in a backplane to support high fan-out may be prohibitively costly. To incorporate more innovative backplane protocol using multi-wavelength will require tunable laser and detectors, which is another costly item [9]. However, innovative approaches to incorporate such components will emerge with time either by discovering new components or fabrication technology, which are cheaper or by using fewer hardware in a system.

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